REMARKS

Prior to the present amendment and response, claims 1, 3-12, 14-15, and 17-23 were pending in the present application. By the present amendment and response, independent claims 1 and 14 have been amended to overcome the Examiner's objections. Thus, claims 1, 3-12, 14-15, and 17-23 remain in the present application. Reconsideration and allowance of pending claims 1, 3-12, 14-15, and 17-23 in view of the above amendments and the following remarks are requested.

A. Objection to Claims 1 and 14

The Examiner has objected to claims 1 and 14 as containing informalities. Applicant has amended claims 1 and 14 and respectfully requests that the informality objection to claims 1 and 14 be withdrawn.

B. Rejection of Claims 1, 3-12, 14-15, and 17-23 under 35 USC §103(a)

The Examiner has rejected claims 1, 3-12, 14-15, and 17-23 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,436,177 to Chiara Zaccherini (hereinafter "Zaccherini") in view of U.S. patent number 5,489,547 to Erdeljac et al. (hereinafter "Erdeljac") and U.S. patent number 6,156,602 to Shao et al. (hereinafter "Shao"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao, singly or in any combination thereof.

The present invention, as defined by amended independent claim 1, recites, among other things, sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, removing a doping barrier, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate. As disclosed in the present application, a first dopant (e.g. an N type dopant) is implanted in a gate region of a polycrystalline layer at a first dose, while a doping barrier prevents the first dopant from being implanted in a resistor region of the polycrystalline layer, where the gate region is situated over a well and the resistor region is situated over a field oxide region, which is not situated over the well. As disclosed in the present application, the well and the field oxide region are formed in a substrate.

As disclosed in the present application, after the doping barrier is removed, a second dopant (e.g. a P type dopant) is implanted in the polycrystalline layer at a second

dose, which determines the resistivity of a resistor subsequently formed in the resistor region of the polycrystalline layer. The first dose of the first dopant is substantially higher than the second dose of the second dopant such that the second dose of the second dopant does not affect transistor gate electrical properties. For example, the first dose of the first dopant can be approximately $6.5x10^{15}$ atoms per square centimeter while the second dose of the second dopant can be approximately $1.0x10^{15}$ atoms per square centimeter. As disclosed in the present application, after a high resistivity resistor has been formed in the resistor region of the polycrystalline layer, P+ doped regions are formed by heavily doping uncovered portions of the resistor region of the polycrystalline layer with a third dopant (e.g. a P type dopant) having the same conductivity type as the second dopant, and silicide contact regions are then formed over the P+ regions. As a result of the above sequential fabrication process steps, the present invention advantageously achieves a high resistivity resistor having a low fabrication cost and improved electrical connectivity.

In contrast to the present invention as defined by amended independent claim 1, Zaccherini does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and

fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate. Zaccherini specifically discloses forming polycrystalline layer 7 over field oxide 5 and channel region 4, where field oxide 5 and channel region 4 are situated on epitaxial layer 3, which covers substrate 2. See, for example, column 2, lines 54-55, column 3, lines 1-14, and Figure 3 of Zaccherini.

However, Zaccherini fails to teach, disclose, or suggest forming a well in substrate 2. Thus, Zaccherini fails to teach, disclose, or remotely suggest forming a layer over a transistor gate region and a field oxide region, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region ant the well are situated on a substrate, as specified in amended independent claim 1. Thus, Zaccherini requires an additional layer (i.e. epitaxial layer 3) to be grown on substrate 2 prior to forming field oxide 5. Thus, by requiring epitaxial layer 3 to be grown on substrate 2, the structure disclosed in Zaccherini is substantially different than the structure as specified in amended independent claim 1. Furthermore, Zaccherini provides no motivation for providing a field oxide region and a well in a substrate, as specified in amended independent claim 1.

Also, in Zaccherini, an N type dopant at an implant dosage of between $5x10^{14}$ and $1x10^{16}$ ions/cm^2 can be implanted in polycrystalline layer 7 directly over channel region 4, while resistors 8 are doped with a P type dopant at an implant dosage of between $1x10^{12}$ to $1x10^{15}$ ions/cm^2. See, for example, Zaccherini, column 3, lines 24-36 and 45-53. Thus, since the implant dosages of the N type dopant and the P type dopant overlap, Zaccherini fails to teach, disclose, or suggest doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, as specified in amended independent claim 1.

Furthermore, Zaccherini states that "[t]he final step of the process according to the present invention is a step of doping the resistors 8 by implantation as shown in FIG. 6." Column 3, lines 45-47 of Zaccherini. Thus, Zaccherini fails to teach, disclose, or remotely suggest forming a silicide blocking layer over the layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, then doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and, next, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as specified in amended independent

claim 1. Moreover, Zaccherini fails to provide any motivation for sequentially performing the above steps as specified in amended independent claim 1. Thus, in sum, Zaccherini fails to teach, disclose, or remotely suggest performing the particular sequence of steps as specified in amended independent claim 1.

In contrast to the present invention as defined by amended independent claim 1, Erdeljac does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate.

Erdeljac specifically discloses forming second polysilicon layer 28 over gates 24 and field oxide regions 20. See, for example, column 2, lines 5-19 and Figure 2 of Erdeljac. In Erdeljac, resistors 32, 34, and 56 are formed in second polysilicon layer 28 on field oxide region 20 that is situated over P- epitaxial layer 12, and gate 24 is formed

in a first polysilicon layer over N well 18, which is formed in P- epitaxial layer 12. See, for example, column 1, lines 39-41, column 2, lines 1-6 and 34-36, and Figure 11 of Erdeljac. However, in Erdeljac, P- epitaxial layer 12 is formed on P+ substrate 10 and N well 18 is formed in P- epitaxial layer 12. See, for example, column 1, lines 31-41 and Figures 1 and 2 of Erdeljac. Thus, fails to teach, disclose, or remotely suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in amended independent claim 1.

Additionally, in Erdeljac, resistors 32, 34, and 56 are formed in second polysilicon layer 28, which is deposited over gate 24, while gate 24 is formed in the first polysilicon layer. Thus, Erdeljac fails to teach, disclose, or remotely suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, as specified in amended independent claim 1.

Furthermore, Erdeljac fails to teach, disclose, or remotely suggest forming a silicide blocking layer over the layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, then doping an outer portion of the layer over the field oxide region with a third

dopant having the second conductivity type, and, next, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as specified in amended independent claim 1. Thus, Erdeljac fails to cure the basic deficiencies of Zaccherini discussed above.

Moreover, the fabrication method and resulting structure disclosed in Erdeljac is substantially different than the fabrication method and resulting structure disclosed in Zaccherini. For example, Zaccherini discloses forming a P doped resistor and a gate terminal in the same polycrystalline layer (i.e. polycrystalline layer 7). In contrast, as discussed above, Erdeljac discloses forming gate 24 in a first polysilicon layer while forming resistors 32, 34, and 56 in a second polysilicon layer (i.e. second polysilicon layer 28). As such, Applicant respectfully submits that there is insufficient motivation for the combination of Zaccherini and Erdeljac as suggested by the Examiner.

In contrast to the present invention as defined by amended independent claim 1, Shao does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the

second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate.

Shao specifically discloses performing N+ implant 18 into poly 2 layer 16 to form the conductivity level of an NMOS poly gate (NMOS gate 40) and also to control the value of a load resistor (i.e. load resistor 38), which is also formed in poly 2 layer 16 over field oxide region 12. See, for example, column 5, lines 7-26 and Figures 1 and 5 of Shao. In Shao, NMOS gate 40 and load resistor 38 are both situated over substrate 10. See, for example, Figure 5 of Shao. Also, Shao fails to teach, disclose, or suggest a well formed in a substrate. Thus, Shao fails to teach, disclose, or remotely suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in amended independent claim 1.

Additionally, in Shao, N+ implant 18 is used to dope poly 2 layer 16, which is subsequently patterned and etched to form load resistor 38 and NMOS gate 40. Thus, in Shao, fails to teach, disclose, or remotely suggest sequentially forming a doping barrier above a layer over a field oxide region, doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, removing the doping barrier, and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, as specified in amended

independent claim 1. Furthermore, Shao fails to teach, disclose, or suggest forming a silicide blocking layer over the layer over the field oxide region after doping the layer over the transistor gate region and the field oxide region with a second dose of the second dopant, then doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and, next, fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, as specified in amended independent claim 1.

As discussed above, amended independent claim 1 recites a series of steps that are performed in a specified sequence that is not disclosed, taught, or suggested in Zaccherini, Erdeljac, and Shao, singly or in any combination thereof. Thus, for the above reasons, Applicant respectfully submits that the combination of Zaccherini, Erdeljac, and Shao suggest by the Examiner does not and cannot result in the present invention as defined by amended independent claim 1. Also, as discussed above, the fabrication steps disclosed in Zaccherini are significantly different from the fabrication steps disclosed in either Erdeljac or Shao. Furthermore, the sequence of steps disclosed in Zaccherini is significantly different than the sequence of steps disclosed in either Erdeljac or Shao. As such, the resulting structure formed in Zaccherini is significantly different than the resulting structure formed in either Erdeljac or Shao. Thus, Applicant respectfully submits that there is not sufficient motivation for modifying Zaccherini in view of Erdeljac, and Shao as suggested by the Examiner. Thus, Applicant respectfully submits

that the combined teachings suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of Applicant's disclosure, which is impermissible.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao, singly or in any combination thereof. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 3-12 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Amended independent claim 14 recites similar limitations as amended independent claim 1 discussed above. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claim 14, is also not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao. As such, the present invention, as defined by amended independent claim 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 15 and 17-24 depending from amended independent claim 14 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 14, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 3-12, 14-15, and 17-23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 3-12, 14-15, and 17-23 pending in the present application is respectfully requested.

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Respectfully Submitted,
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